**ECE 324 Homework 4: Shift Register Simulation**

Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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| **Exercise** | **Course outcome** | | **Grade** |
| Homework4 | | 2.a, 7.b | /30 |

2.a. Define engineering problems from specified needs for digital systems including implementation on FPGAs using HDL programming.

7.b. Employ appropriate learning strategies such as communicating with an expert, using external resources, experimentation, simulation, etc.

# Learning Objectives

1. Practice writing a sequential SystemVerilog testbench.
2. Use logic simulation to verify functional correctness of a sequential circuit.

# Exercise

1. Write a SystemVerilog testbench for Pong Chu’s Universal Shift Register module (Listing 4.10) included in the HW4 folder (note all of Pong Chu’s textbook code can be downloaded from Blackboard 🡪 ECE 324 🡪 Course 🡪 Content 🡪 Term Project 🡪 Chu SystemVerilog Source Files). The testbench will instantiate the USR, redefining its parameter to N = 4, generate a clock signal, and apply a stimulus sequence to the USR inputs. Use the testbench clock to control when the stimulus signals change. Use Chu’s *Testbench for a universal binary counter* (Listing 4.14) as an example.

The stimulus sequence should test and verify the following functions:

* 1. load
  2. no op (hold)
  3. shift left 4 places
  4. shift right 4 places
  5. asynchronous reset

1. Simulate using Vivado.
2. Submit the following for grading by uploading it to the drop box on Blackboard:
   1. The SystemVerilog testbench that you wrote. The SystemVerilog code should include comments that explain how it works.
   2. Screenshot(s) of the simulation results proving that your module functions correctly. Make sure that signal name and time labels are legible in all screenshots.
   3. A written report that explains how your simulation results prove that that the USR functions correctly. Please attach the provided cover sheet to your report.